Reference:

Sedra, A., & Smith, K. (n.d.). Microelectronic circuits (4th ed., The Oxford series in electrical engineering). New York: Oxford University Press.

**Metal Oxide Semiconductor Field-Effect Transistor (MOSFET)**

Field-Effect transistors (FET) are voltage-operated devices. They use electric field to control device conductivity. Most common are Metal Oxide Semiconductor FETs (MOSFETs), also known as MOS transistors.

[Intro]

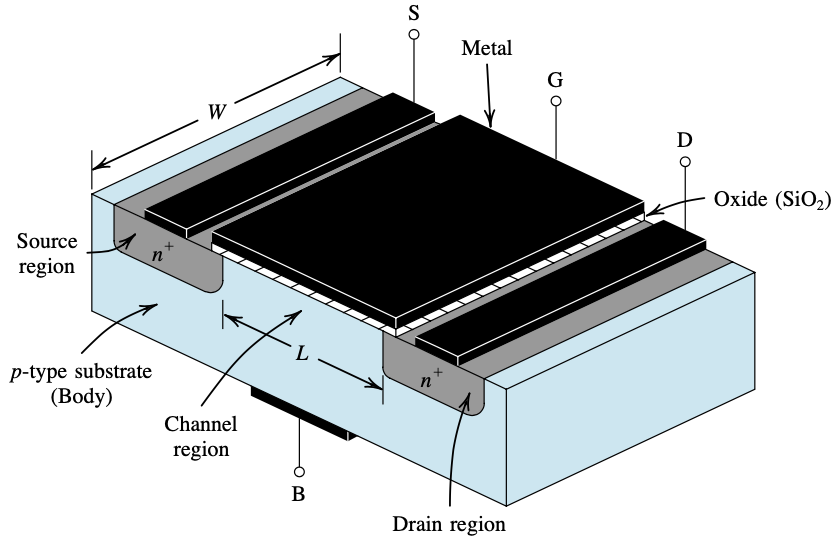
**Structure**

The structure of a MOSFET is illustrated in fig??. The nMOS transistor is realized on a body of p-type silicon substrate. Two regions of the substrate, called source region and drain region, are heavily doped with n+ silicon. Between the n-regions a silicon dioxide (SiO2) layer is grown on top of the substrate. A metal gate electron is deposited on top of the oxide layer. Ohmic contacts are attached to source and drain region, as well as the substrate.

Where an n-region interfaces with the p-type silicon body a pn-junction forms. Source and drain region are separated by the highly resistive substrate and initially resemble two diodes. The area between source and drain region is referred to as “channel-region”.

The substrate electrode (B) is grounded and is not considered a functional terminal of the MOSFET. The transistor is there for referred to as a three-terminal device, where the terminals are source (S), drain (D) and gate (G).

The basic transistor composition is symmetrical. “Source” and “drain” merely indicate which terminal supplies (source) and which collects (drain) charge carriers. Conventional current flows from drain to source. Adjusting input voltage to the gate terminal alters device conductivity. *Voltages applied to the device are relative to source terminal.*



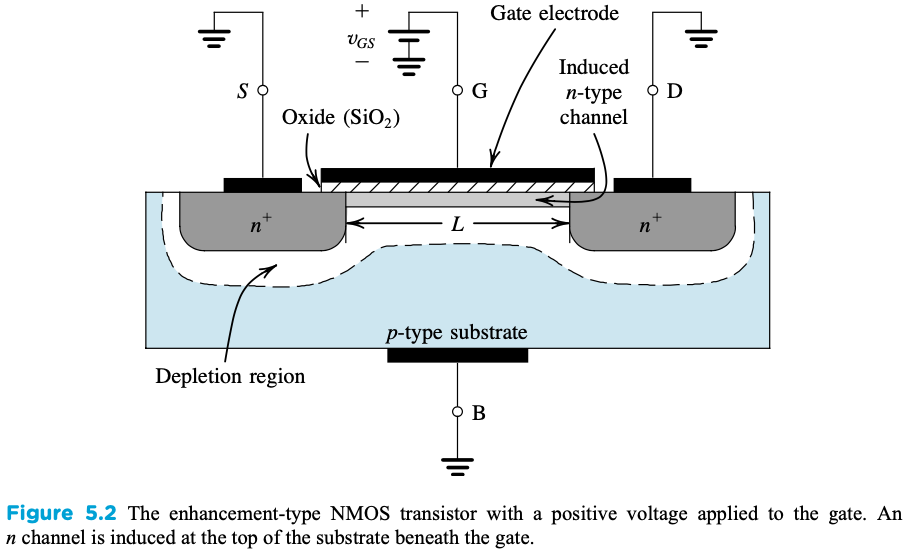
**Zero gate-to-source voltage,**

Without any voltage difference between gate and source the transistor in fig?? simply resembles two diodes, between which no electricity flows. The channel-region is highly resistive and does not permit charge carriers of the source-region to travel to the drain-region.

**Channel formation**

In order for current to flow between the source and the drain terminals an electrical connection must be made between the two. Increasing up to or beyond a threshold voltage (which is determined during fabrication) generates a conducting channel between S and D terminal. Voltage applied to gate gives rise to an electric field in the oxide layer. In the nMOS, a positive V\_GS pushes holes (charge carriers of the substrate) downwards and leaves bound electrons of acceptor atoms exposed. Furthermore, the electric field pulls abundant electrons from the n-regions into the channel-region. With sufficiently large gate voltage $()$, enough electrons accumulate across the substrate-oxide interface to invert a thin layer of the p-type substrate into n-type. The inversion layer, also referred to as the n-channel. It connects source-region to drain-region such that charge carriers can flow from one end to the other.

Any additional voltage increase beyond threshold extends the channel deeper into the substrate. The overdrive voltage (OV) is defined as in []. Raising V\_OV increases channel charge proportionally. With more available carriers the device conductivity has increased.



**Drain-to-source voltage, $**

Assuming applied gate voltage is above critical threshold, electrons can flow freely between n-regions though the channel. The relationship between drain current i\_D and drain-to-source voltage v\_DS is depicted in fig??. Without any voltage ($$) to coach the electrons in a specific direction the channel current is zero (i\_D=0). This can be changed by introducing a small positive potential drop across the channel which promotes electron flow from source to drain. Slowly raising V\_DS increases the current linearly.

Proceeding to larger voltages the growth of i\_D slows because of increasing channel resistivity. When V\_DS approaches V\_TH the channel feels a notable negative potential drop across terminals S and D and becomes asymmetrical. Because of this potential the channel tapers off linearly; thickest near the source- than the drain-end

A picture containing clock

Description automatically generated

Current continuously increases with V\_DS in the interval [0,V\_OV], proportionally for low V\_DS and less than linear as the voltage approaches V\_OV.

Increasing more…

Pinched off

Lowers resistivity

Current increase slows down

Voltage across channel appears as a potential drop. The voltage near source end is larger than voltage near drain end. The force pulling electrons from drain to channel-region is weaker than that on the opposing end. Consequently the channel thickness appears to taper off, being thicker at source- than at drain-channel interface.

Note that conventional current flows against the electron flow. From now on, the term “current” refers to the flow of charge carriers and it should not be confused with conventional current, which flows in the opposite direction.

At this point conventional current leaving drain and received by source are the same (i.e. $i\_s = i\_D$). The gate electrode is electrically isolated from the n-channel and gate current is thus zero ($i\_G=0$).

**A close up of a map

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**Drain-to-source voltage, $**

Up to V\_OV the channel gradually increases resistivity and drain current is less effectively amplified with V\_DS. Beyond overdrive voltage current becomes independent of V\_DS. Channel current depends on how fast charge carriers within travels (I = dq/dt). Sped up by V\_DS, charge carriers eventually reach maximum velocity (i.e. saturation velocity) [R. Jacob Baker]. The current is constant with V\_DS and can only be amplified by increasing V\_GS.

**Saturation mode**

Increasing V\_DS gradually increases channel resistivity. The applied voltage appears as a voltage drop across the channel. Voltage decreases from the source end to the drain end. Because of this the channel becomes asymmetrical, thickest near the source-channel interface and gradually tapering off as it approaches the drain. The drain end appears “pinched-off”. As V\_DS steadily increases the channel thickeness near drain keeps shrinking and channel resistivity increases even further.

once channel causes channel resistance to the current stops increasing linearly with V\_DS the channels conductivity has started to increase. effectively experiences a potential drop from between source and drain. appears as a voltage drop across the channel. The voltage decreases from source to drain As V\_DS approaches the overdrive voltage channel resistane increases.the drain current remains constant.

channel gradually becomes more and more asymmetrical. The asymmetry is caused by a The increased voltage drop across the channel causes

**we are increasing drain-to-source voltage. The gate-source voltage and gate-drain voltage are different. Consequently channel depth decreases, being thicker at source end interface than drain end.**

**Come back to later…**

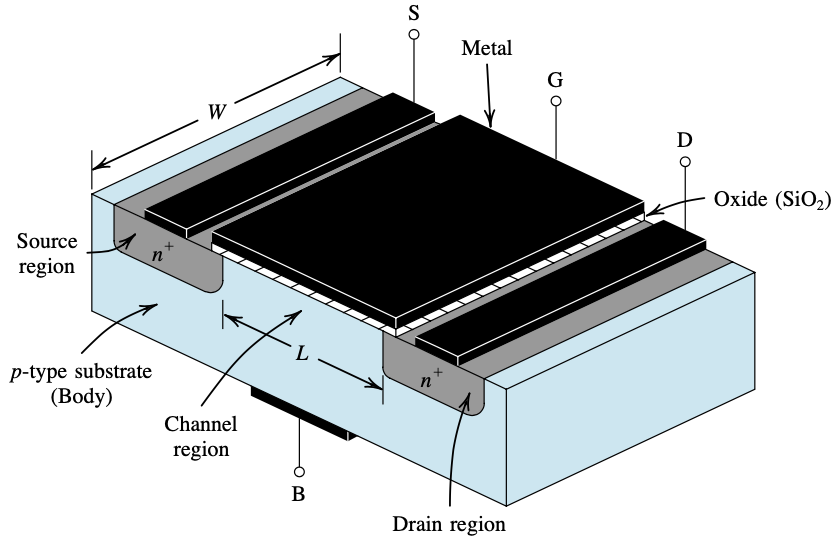
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**Metal Oxide Semiconductor Field-Effect Transistor (MOSFET)**

Field-Effect transistors (FET) are voltage-operated devices. They use electric field to control device conductivity.

Most commonly used are Metal Oxide Semiconductor FETs (MOSFETs), also known as MOS transistors. MOS transistors (fig??) act as highly resistant capacitors. They composite three basic layers. On the bottom, a silicon substrate on which a silicon oxide (SiO2) structure is grown. Attached to the thin oxide layer is an even thinner metal gate electrode. SiO2 is a dielectric and electrically isolates gate from substrate; current from substrate to gate is prohibited. The metal-oxide-semiconductor sandwich resembles a capacitor with nearly infinite resistance.

Sections of the substrate are carved out (oxidized) and two **wells** are left behind. The wells are filled with silicon type oppositely doped from substrate. Illustrated in figure ?? are two types of MOS transistors. **pMOS** transistors are of n-type substrate and hold p-wells. Inversely, **nMOS** transistors are made of p-type substrate and n-wells. **Charge carriers** are either electrons or holes, but never both; pMOS transport electrons while nMOS transport holes.

nMOS transistor


[Sedra, A., & Smith, K.]

MOS transistors have three terminals, namely source, drain and gate. **Gate** (G) terminal is part of the metal electrode attached to oxide layer. **Source** and **drain** are connected to the wells through ohmic contacts. Substrate is connected to ground and is not considered a terminal.

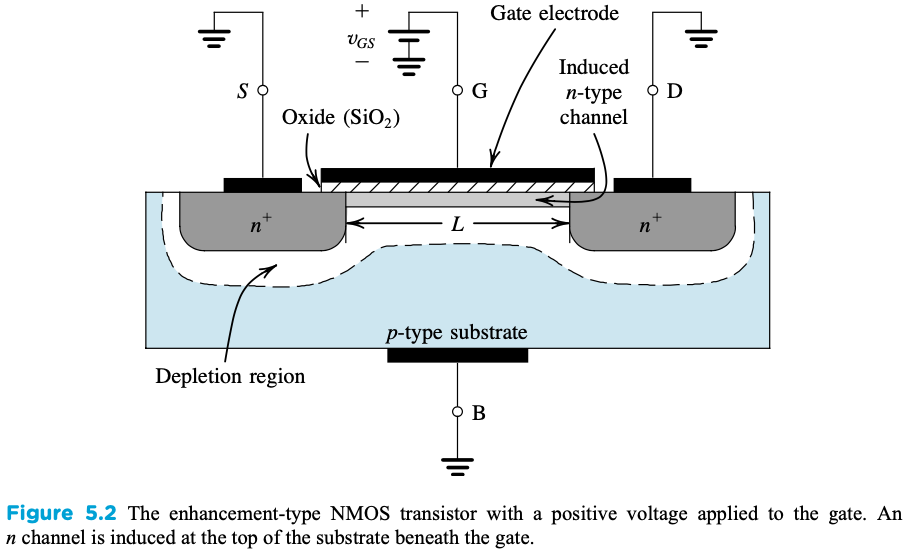
Voltage can be applied to the terminals and alter conductive properties of the transistor. Voltages are in respect to source terminal. Initially, **drain-to-source voltage V\_DS** is zero and so is the current between the two terminals.

When a small **voltage** is applied to **gate** an electric field occurs between capacitor plates, gate and substrate. Charge carriers are attracted to gate and the depletion region grows. Because of the insulation oxide layer charge carriers are not collected by gate and accumulate across substrate-oxide interface.

At **threshold voltage** V\_TH substrate becomes partially inverted near the interface. The thin inversion layer is a **conducting channel** that electrically connects S to D.

When V\_DS>0 current flows from source to drain and is proportional to gate-to-source voltage V\_GS. (No current ever flows to gate, I\_G = 0).

Increasing voltage at drain (V\_D) creates an uneven field across the channel. When $V\_{DS} >= V\_{GS} -V\_{TH}$ the channel is **pinched-off** near drain and current grows less than linear with V\_DS.



^rewrite

**Operation Modes**

Three basic modes of MOS and their conditions are listed in table??.

The transistor is in **saturation mode** when V\_{ DS } = V\_{ DSsat } = V\_{ GS } -V\_{ TH }. Charge carriers are sped up by V\_DS to a point where they reach carrier velocity saturation (i.e. maximum velocity) [R. Jacob Baker]. At this point, current is constant with V\_DS and can only be amplified by increasing V\_GS.

With V\_GS below threshold voltage the transistor in cutoff mode and does not conduct any electricity (i\_G=i\_S=i\_D).

Triode mode?

Adjusting input voltage to gate manages device conductivity. The **gate-source voltage V\_GS** causes up rise of an electric field between capacitor plates, gate and substrate. Charge carriers are attracted to gate. Because of the insulating oxide layer, charge carriers are not collected by gate and accumulate across substrate-oxide interface. At threshold voltage V\_th substrate becomes partially inverted near the interface. The thin inversion layer is a channel that electrically connects source and drain. Voltage increase beyond critical threshold (V\_GS>V\_TH) thickens the connecting channel and makes room for larger streams of charge carriers. I.e., increasing gate voltage **amplifies current**.

Voltage can also be applied to source/drain. Doing so generates an electric field between S and D and causes the channel to retract away from the drain. The channel becomes asymmetrical, its thickness tapers off as it approaches D (fig. ??). Beyond ?? Increasing drain-source voltage (V\_DS) ~~can~~ completely disconnect the channel from drain. Though S and D are no longer directly connected, current can still flow. Between the “pinched off” channel tip and drain there is a depleted area where charge can drift with respect to the electric field. While a uniform channel permits current in both directions, the disconnected asymmetrical channel is unidirectional. This mode of operation is called **saturation mode**.

In saturation mode, further increase of V\_DS does not cause current to increase. Electrons are sped up by V\_DS to a point where they reach carrier velocity saturation (i.e. maximum velocity) and the current is said to be saturated and constant. [R. Jacob Baker] At this point, raising gate-source voltage can be used to amplify the current.

**CMOS technology and circuit logic**

Complementary metal–oxide–semiconductor (CMOS) is a fabrication method used to integrate transistors on a piece of semiconductor, usually silicon. ~~MOS is a type of transistor fabricated by the oxidation of a semiconductor.~~

In pMOS transistors, **source** (S) and **drain** (D) are connected to p-wells in an n-type substrate. Inversely, in nMOS transistors, source and drain are connected to n-wells in a p-type substrate.

The gate-source voltage V\_GS controls the conductivity over the transistor. The potential difference gives rise to an electric field between gate and substrate.

In nMOS, a positive voltage (with respect to ??) attracts substrate electrons to gate and pushes holes away. With sufficient magnitude gate-source voltage can cause partial inversion, turning a fraction of the p-doped substrate into n-type. This creates an n-channel (hence nMOS) connecting source and drain and allows electron flow between the two. Increasing V\_GS thickens the channel and opens up for greater electron current, increasing conductivity. Similarly, negative gate-source voltage can be applied to pMOS to create a p-channel. Charge carriers of nMOS and pMOS are electrons and holes, respectively.

A voltage can also be applied such that an electric field occurs between source and drain. In nMOS, (a pos/neg voltage with respect to ??) causes the n-channel to retract away from the drain. The channel becomes asymmetrical, its thickness tapers off as it approaches D (fig. ??). Increasing drain-source voltage (V\_DS) can completely disconnect the channel from drain. Though S and D are no longer directly connected, current can still flow. Between the “pinched off” channel tip and drain there is a depleted area where charge can drift. While a uniform n-channel permits current in both directions, the disconnected asymmetrical channel is unidirectional. This mode of operation is called *saturation mode*.

In saturation mode, further increase of V\_DS does not cause current to increase. Electrons are sped up by V\_DS to a point where they reach *carrier velocity saturation* (i.e. maximum velocity) and the current is said to be saturated and constant. [R. Jacob Baker] At this point, raising gate-source voltage can be used to amplify the current.

In a circuit, a saturated MOS transistor works like a switch, current either flows (switch ON) or doesn’t (switch OFF). If input voltage applied to G is high, an n-channel forms in nMOS and current passes though, the switch is “ON”. In pMOS, a high input voltage does not create a p-channel and no current passes the transistor, the switch is “OFF”. Reversely, a low voltage turns nMOS “OFF” while pMOS “ON”.

A close up of a map

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Operation? Effects of this??

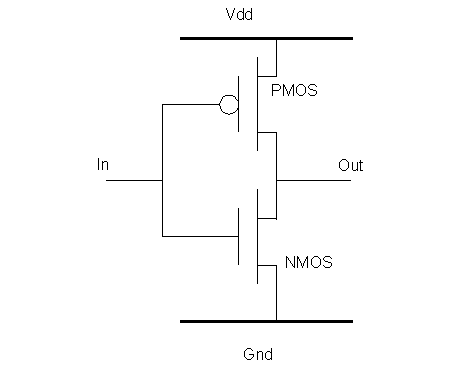
In saturation mode the transistor works as a switch. The current is either ON or OFF. [[\*](https://onlinelibrary.wiley.com/doi/pdf/10.1002/9780470891179), double check source]

By controlling device conductivity, electronical signals can be amplified or switch on/off. (“wiki”) The combination of the complementary **pMOS** and **nMOS** semiconductors in a circuit, create a **CMOS** transistor (pMOS + nMOS = CMOS) as shown in Fig. ??.

Logics of CMOS

Perks

A close up of a clock

Description automatically generated

A screen shot of a clock

Description automatically generated

**PIXEL SENSORS**

A pixel sensor is an **imaging sensor** and was in early days limited to **light applications**. In later years pixel sensors have been developed to also detect **energetic particles**.

The smallest sensing unit of a pixel sensor is a **pixel**. A matrix of pixels forms a larger sensing area and together with the proper stimulus (light or ionizing particles) they generate an image. Image **granularity** (spatial resolution) is determined by the pixels size; a large pixel gives low granularity, few pixels fit in a matrix, and a small pixel gives high granularity, many pixels fit in a matrix. The sensitive mechanism of a pixel is a configuration of semiconductors which generate a pulse signal as a consequence of ionizing radiation traversing its sensing volume.

There are two types of pixel sensors, active and passive. The main difference between an **Active Pixel Sensor** (APS) and a **Passive Pixel Sensor** (PPS) is that the former incorporates one or more amplifying transistor (MOSFET transistors) while the latter does not. Pixels of PPS are read out without amplification. Transistors in an APS convert generated charge to voltage, amplify the voltage signal and remove noise. These characteristics make APS superior to PPS which has high noise and slow readout rates in comparison.

**MAPS**

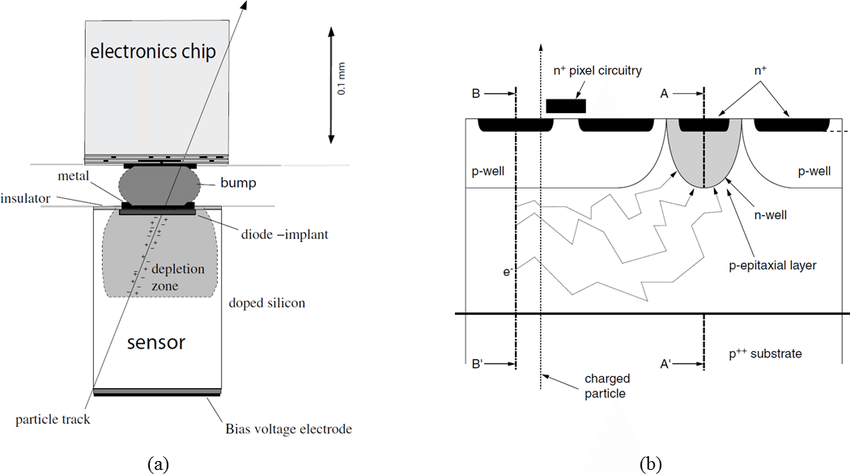
In the early 1990s, APS based on CMOS technology was proposed and at the end of the decade so was their application in particle physics [R.Turchetta ]. CMOS based APS implement a monolithic pixel architecture (Fig.??b). Monolithic designs include in-pixel circuitry and provide a compact sensor-electronics configuration. In contrast, a **hybrid** **architecture** (Fig.?? a) constitutes of individually manufactured pixel and readout electronics coupled by the means of bump bonding.

Monolithic APS (MAPS) architecture allows for pixel integrated circuitry, which avoids complexities brought by bump bonding and waste of pixel area due to extra material. MAPS also show significantly lower power consumption of , … (4mW/cm” ish) SOURCE??

while hybrids :few hundred mW/cm2[L.Maczewski].

Small pixels, more functionality

?? Other great interests of MAPS are its low power consumption and low cost …



Sources

[L.Maczewski] MAPS (used by Viljar): https://arxiv.org/pdf/1005.3710.pdf

Sedra, A., & Smith, K. (n.d.). Microelectronic circuits (4th ed., The Oxford series in electrical engineering). New York: Oxford University Press.

Moved to ALPIDE:

The sensor is realized on a silicon substrate on which a highly resistive epitaxial layer (sensor active volume) is grown. Into the epitaxial layer p-wells are placed. A potential barrier forms where the heavily p-doped (P++) substrate and (P+) p-wells meet the lightly p-doped (P-) epitaxial layer. Electrons (e) are **vertically confined** by the potential barriers and **diffuse laterally** across pixels.

An important feature is the implementation of a **deep p-well** which shields n-wells of pMOS transistor from the active layer. This prohibits diodes and n-wells from competing in charge collection.

N-well diodes are the sensing elements and are surrounded by the depletion volume. Moderate **reverse bias** can be applied to the substrate in order to increase depletion volume and improve charge collection.

Most part of the epitaxial layer is free of electric field. Charge is left to thermally diffuse in the active volume until collected by the diode or it recombines with the atomic structure. Because of this MAPS have slow collection times, approximately 100ns. [[\*](https://arxiv.org/pdf/1005.3710.pdf)]